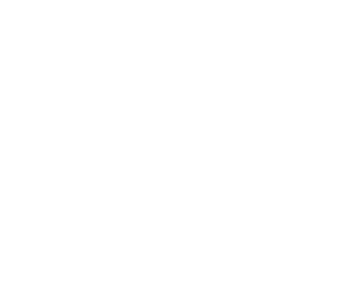
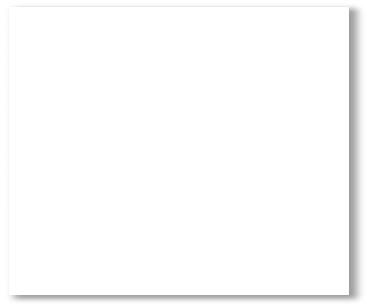
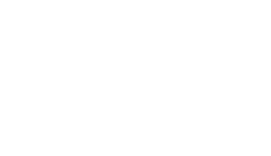
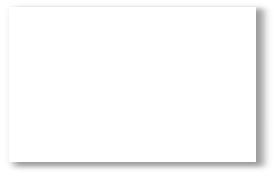
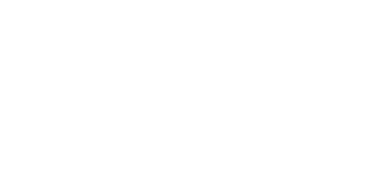
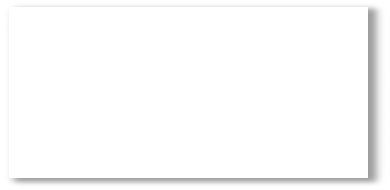
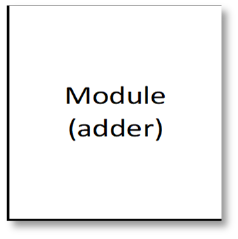
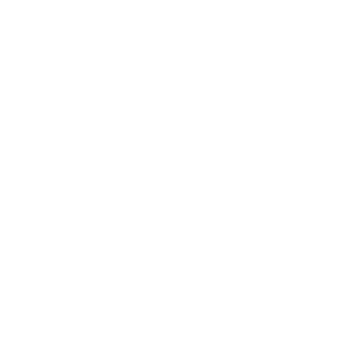
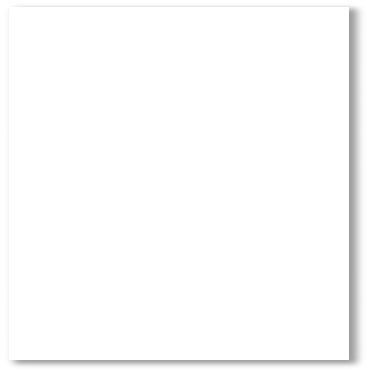
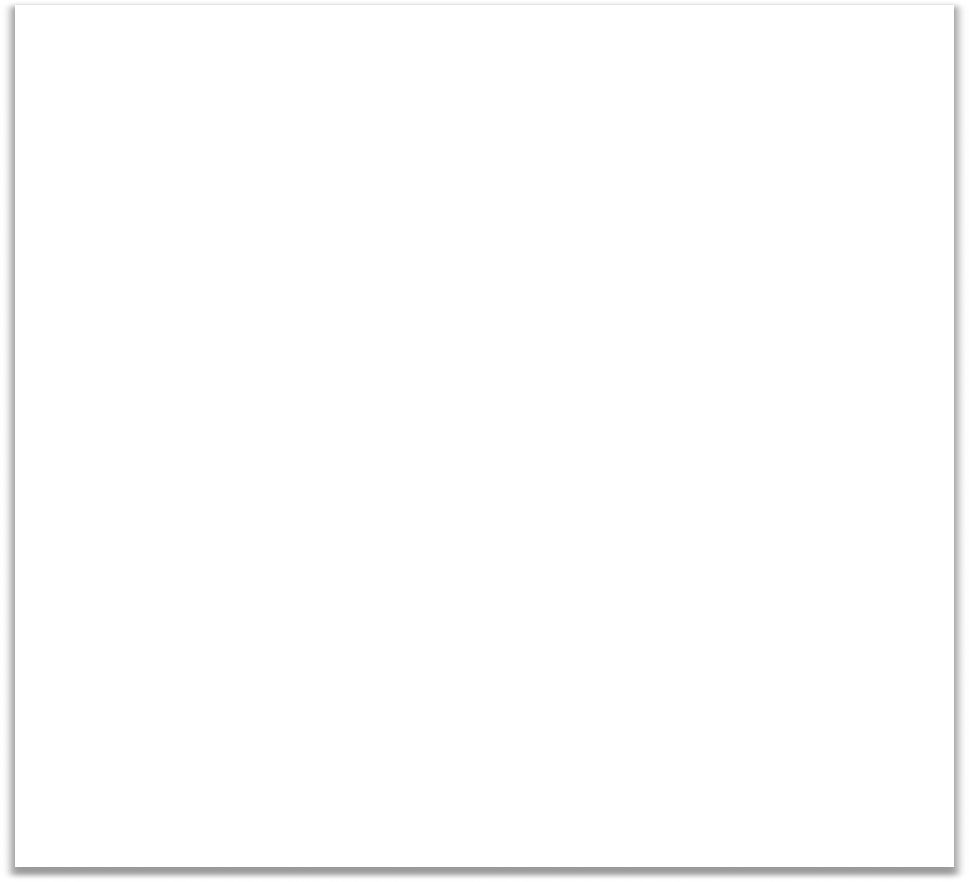
**EEE 525 LAB 4**

**Milestone 1**

# Architecture/High-level Block Diagram:

**Module (gcn)**

clk



Module

(arg\_max)

out\_col\_ready

Module

(aggregate\_fun)

Module

(adder)

element\_out

Module

(mult\_binary)

dff

dff

dff

dff

dff

dff

dff

dff

dff

dff

dff

dff

dff

dff

dff

dff

dff

row\_feature[0]

.

.

row\_feature[n]

row\_weight[0]

.

.

row\_weight[n]

input\_addr\_fm[0]

input\_addr\_fm[n]

Input\_addr\_wm[0]

Input\_addr\_wm[n] Input\_re

COO\_mat

out\_tranform\_col\_final

Rst\_n

y

we

Output\_addr

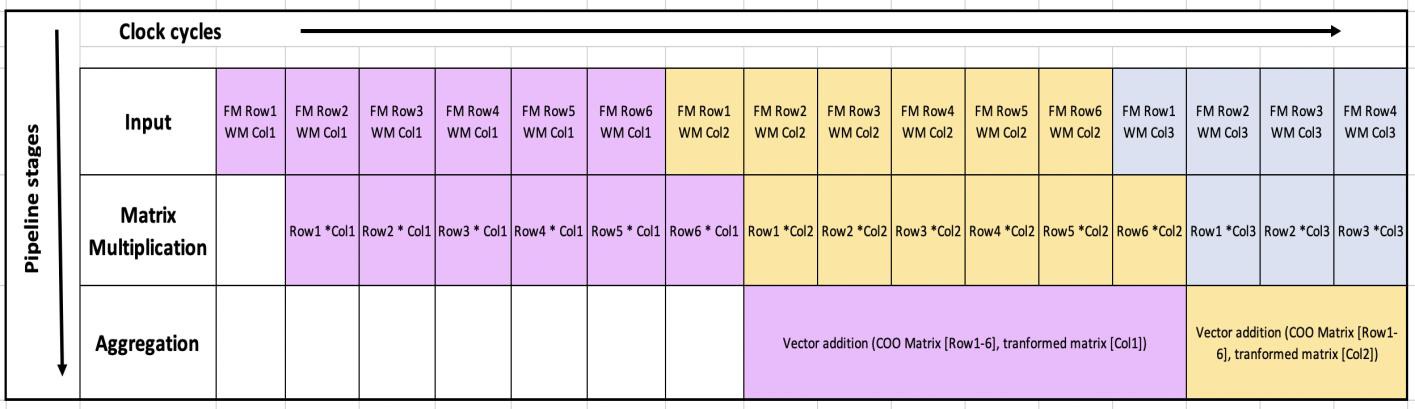
start

done

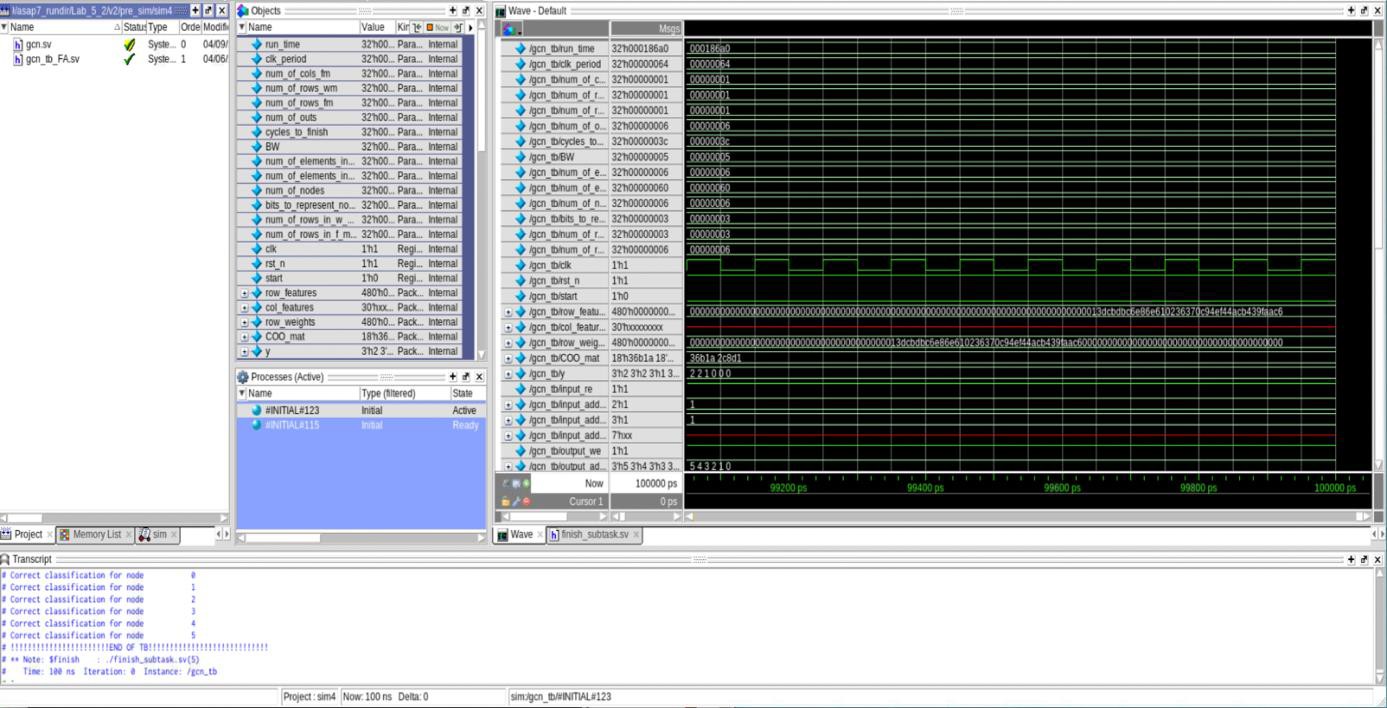
***High-level block diagram***

# Design decisions: (with 1-2 appropriate figures)

We have designed the GCN module for a node classification application as follows:

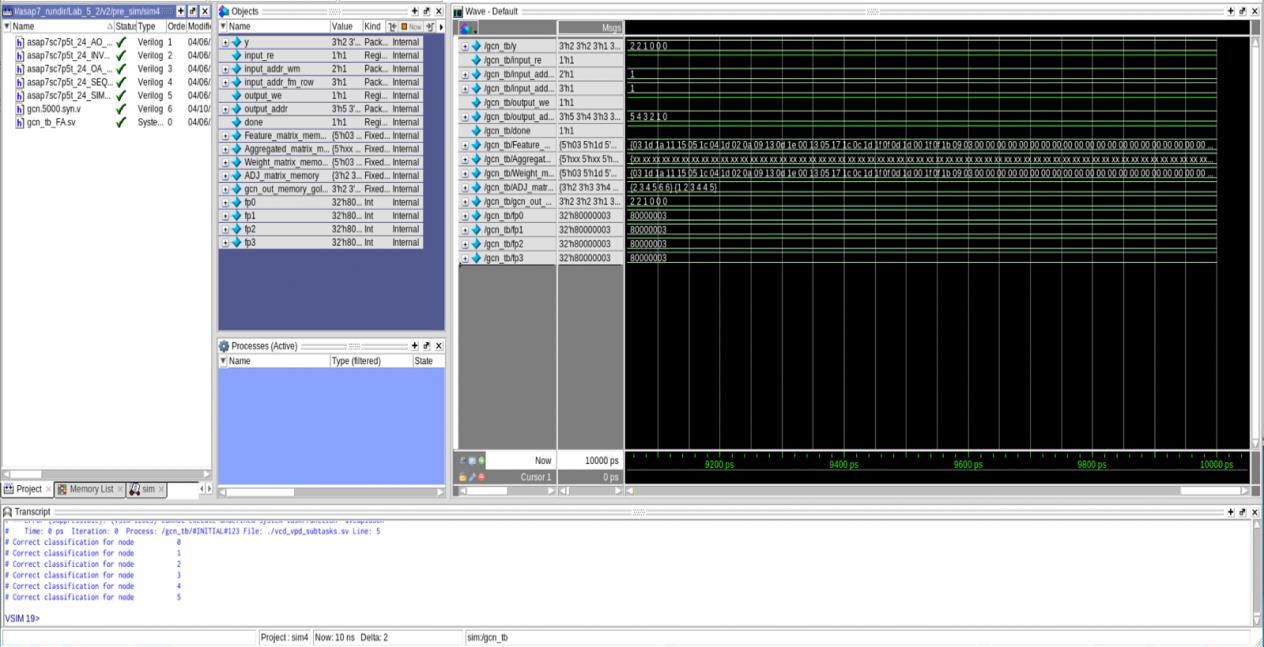
* xxx.
* xxx:
* *Representation of pipeline stages in design*

## Behavioral Verilog – Simulation:



*Correctness of the module with behavioral Verilog*

## Post\_Synthesis – Simulation:

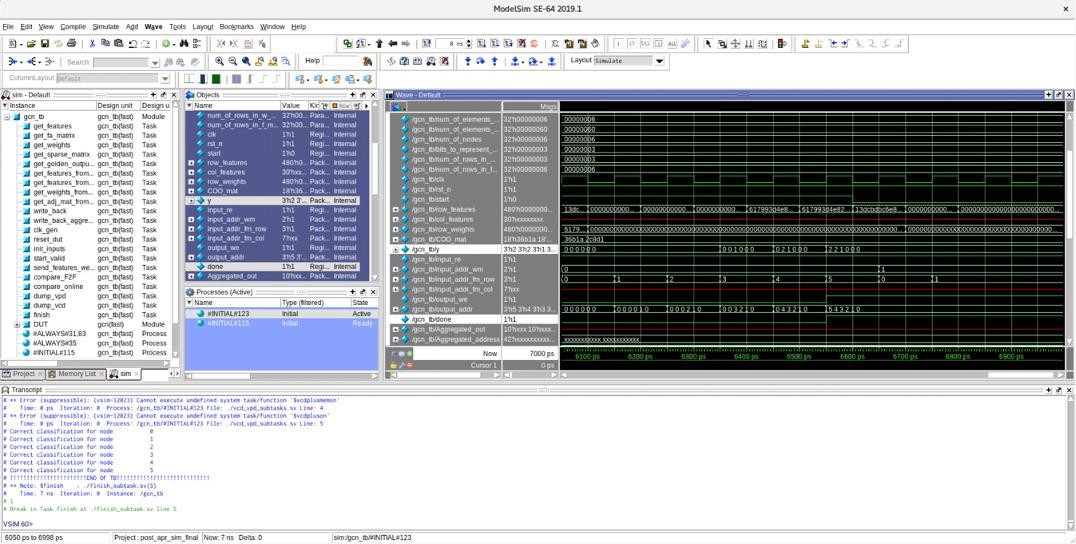


*Correctness of the module with post-synthesis Verilog netlist*

**Milestone 2**

# Total Latency:

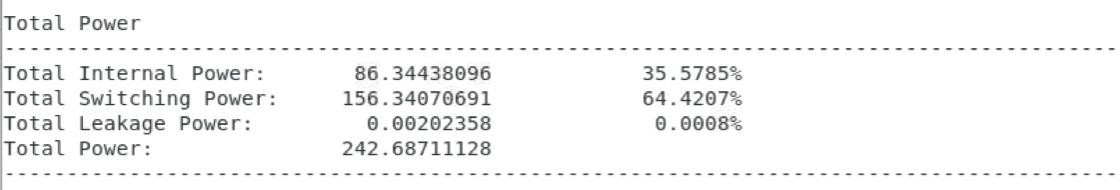
* + Total Latency: **xxx ns**, at the clock frequency of **xxx MHz**.
  + Screenshot of Modelsim:



*post APR simulations screenshot*

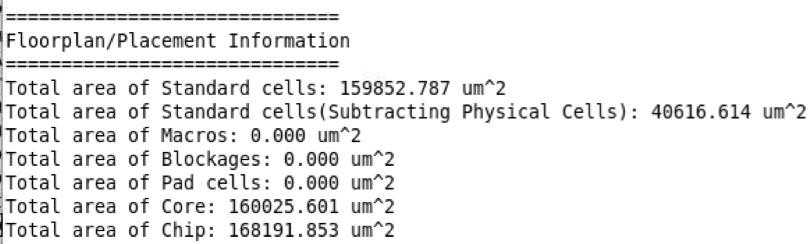
# Power:

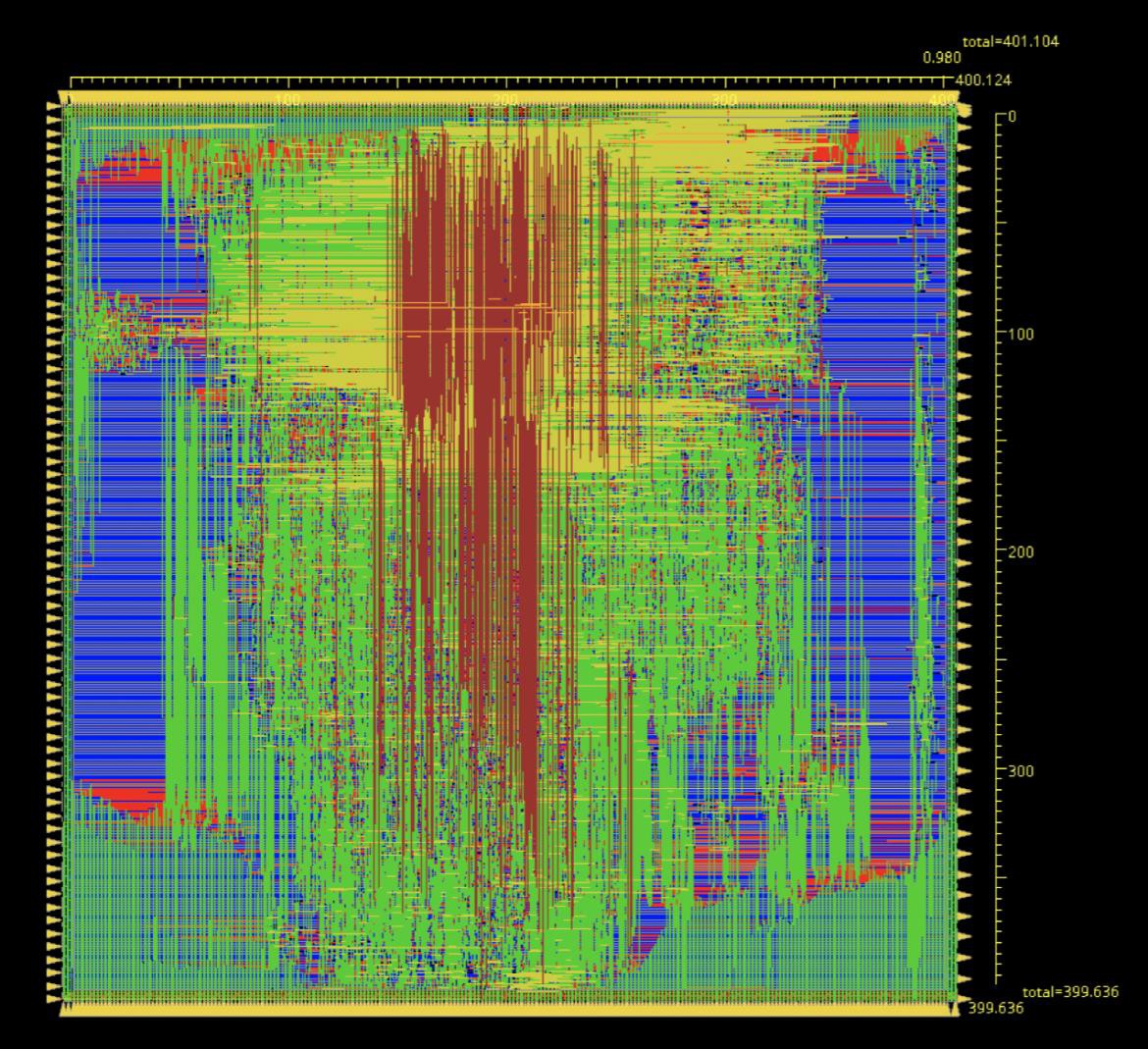
* + Total Power (From Innovus): **xx mW**



# Area:

* + Standard cells + Filler cells: **xxx mm2**

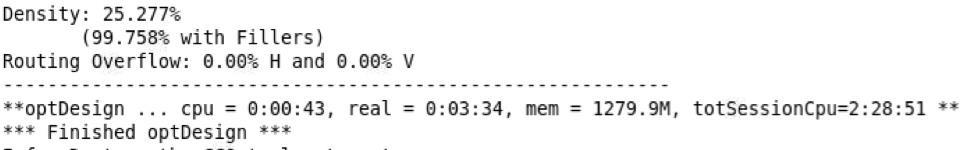


*Snippet from log*

*Design x and y dimensions screenshot*

# Innovus density:

* + Before filler cell insertion: **XXX**



# Number of gates:

* + Gates = **xxx**
  + Cells = **xxx**

## Post\_APR – DRC Check:

**Post\_APR – LVS Check:**

(Submit your geom.rpt and conn.rpt, as well as attach your screenshot of them here)

**Screenshot of your timing report for the worstcase hold and setup path**

One screenshot of the timing report for the worst setup and worst hold. Do not need the top 3 here.

**Note:**

If you have any additional comments, you can briefly document them here.